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A GENERAL USE CIRCUIT FOR AUDIO SIGNAL DISTORTION EXPLOTING ANY NON-LINEAR ELECTRON DEVICE

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ABSTRACT

In this paper, we propose the use of the transimpedance amplifier configuration as a simple generic circuit for electron device-based audio distortion. The goal is to take advantage of the non-linearities in the transfer curves of any device, such as diode, JFET, MOSFET, and control the level and type of harmonic distortion only through bias voltages and signal amplitude. The case of a nMOSFET is taken as a case study, revealing a rich dependence of generated harmonics on the region of operation (linear to saturation), and from weak to strong inversion. A continuous and analytical Lambert-W based model was used for simulations of harmonic distortion, which were verified through measurements.

1. INTRODUCTION

Since the beginning of electrical musical instruments, musicians are trying to achieve a unique sound through their gear with all kinds of effect units. Modulation, reverb, overdrive and distortion effects are widely used for electric guitars but nowadays also by any electric string instrument, synthesizers, keyboards or even vocals. For example, a signal can be distorted through soft or hard clipping, or through any non-linear transfer function, symmetrical or asymmetrical. To achieve all these cases of signal distortion, the typical circuits used are single or multiple gain stages with or without diode clipping. For the gain stages there are hundreds of different combinations that can be used: from vacuum tubes [1], [2] to opamps [3], from silicon to germanium diodes [4], from BJTs to JFETs and MOSFETs [5], [6], each circuit has a different transfer curve and as a result a unique tone character, usually thanks to the devices' non-linear response. Diodes are used for both soft and hard or shunt clipping, in different configurations: in amplifier feedback loop or shunt to ground, respectively. The clipping of the signal can also be symmetrical or asymmetrical, leading to purely odd or odd/even harmonics.

To our knowledge, in all above cases, the non-linear devices are either used as non-linear resistors in an OPAMP's feedback loop or as shunting elements. As a result, only specific amplitude-dependent regions of non-linear response are being exploited. In this work, we propose a method with which one can make use of any non-linear I-V characteristic exploiting various voltage bias regions, while having complete control of the generated harmonics. Despite the fact that there has been an in-depth analysis of harmonic distortion in MOSFETs [7] and even more advanced FET structures [8], [9], it has not yet been used in the configuration that we propose, therefore we chose the MOSFET device as a case study to demonstrate the applicability and advantages of our method.

2. DEVELOPMENT OF THE PROPOSED METHOD

In this section, we present the step-by-step development of the proposed method, presenting the case of a n-channel MOSFET as an example for electron device-based harmonic distortion.

2.1. The transimpedance amplifier as an electron device characterization instrument

The Transimpedance amplifiers (TIA) are widely used to translate the current output of sensors like photodiode-to-voltage signals [10], since many circuits and instruments can only accept voltage input. Moreover, they are used as current preamplifiers in precision measurement instruments such as in current DC and noise characterization [11].

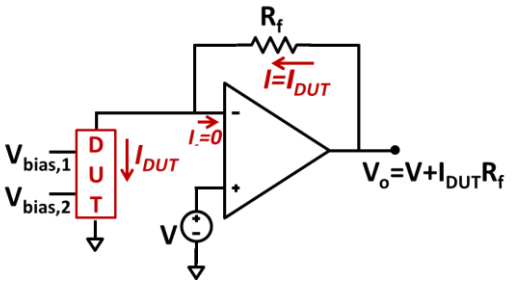

Figure 1: *Typical current-to-voltage converter configuration with transimpedance amplifier for electron device characterization (DC and noise)*

As shown in Fig. 1, the (TIAs) configuration of an operational amplifier (OPAMP) can be used as a current-to-voltage converter

for any device under test (DUT) connected at its input and controlled by various bias voltages (V, V_{bias}). Since the current flowing in the input of the OPAMP can be considered zero, and the negative feedback resistor guarantees the OPAMP's linear regime, the DUT current has to be equal to the current flowing in the feedback loop. Therefore $I_{DUT} = (V_o\text{-}V)/R_f$, because the OPAMP functions in linear mode thus $V_+ = V_-$. So, the output voltage of a TIA would be:

$$V_o = V + I_{DUT}R_f \tag{1}$$

It becomes obvious that the DC voltage output is actually independent of any other device bias voltages other than the one connected to the OPAMP. Of course, it has to be noted that we consider an ideal OPAMP with linear response for a large range of voltage swings and with no input voltage offsets. In a real scenario, one needs to correct the input offset and make sure the output voltage does not exceed the linear response region of the OPAMP, which is directly limited by the supply voltage bias. Fortunately, this can be easily regulated with the value of Rf, so that the output signal is never higher than the maximum allowed limit for linear OPAMP operation. Moreover, a real OPAMP has also a maximum output current above which it also saturates. The latter issue cannot be avoided by adjusting Rf, but only by choosing carefully the OPAMP model so that it can provide the maximum current of the connected DUT.

Now if we consider an AC output after a high-pass filter (HPF) that cuts frequency content below 10 Hz for example, we could approximate the output voltage signal as:

$$v_o = i_{DUT}R_f \tag{2}$$

where iDUT are the current variations of the DUT due to variations in one (or more) of the bias voltages. Therefore the voltage signal of the output is a direct linear function of solely the device AC current, with a gain equal to the feedback resistor value, Rf. An alternative way to obtain (2) without the use of a filter, which could impact the signal's phase at low frequencies, is to connect a voltage subtractor circuit in series with the output, to remove the same DC voltage V that we apply at the OPAMP's (+) input.

Finally, as happens with all analog audio circuits, since both the DUT and the OPAMP have DC/AC characteristics and responses that vary for each copy of the device, some manual tweaking of supply bias and DUT bias may be needed to obtain exactly the same behaviour from one circuit to another identical one.

2.2. Controlling the harmonic distortion through voltage bias and signal amplitude

In the example of Fig. 1, the current flowing through the device under test can be expressed as $I_{DUT} = I(V, V_{bias1}, V_{bias2})$. Therefore, an AC component, v_{in}, is added to one of the bias voltages, and the rest are constant with time, the small-signal AC output of the OPAMP would be:

$$v_0 = \frac{\partial I_{DUT}}{\partial V_{in}} v_{in} R_f = f(V_{in}, v_{in}, V_{bias,1-2}, \dots) \tag{3}$$

where $\frac{\partial i_{DUT}}{\partial V_{in}}$ is a function of the DC bias voltages and corresponds to the 1st order sensitivity of I_{DUT} to V_{in}. This means that the dynamic output response is unique and fully controlled by the choice of signal input and the bias voltages. Now, if we also account for higher order components [7] introduced by a non-linear relation of I_{DUT} with V_{bias}, we obtain:

$$v_0 = R_f \left(\frac{\partial I_{DUT}}{\partial V_{in}} v_{in} + \frac{1}{2} \frac{\partial^2 I_{DUT}}{\partial {V_{in}}^2} {v_{in}}^2 + \dots + \frac{1}{n!} \frac{\partial^n I_{DUT}}{\partial {V_{in}}^n} {v_{in}}^n \right) \tag{4}$$

We can therefore see that with the configuration of Fig. 1, even the generated harmonics that define the distortion levels only depend on the relation between I_{DUT} and the voltage bias where the signal is applied, for the given DC biases.

3. CASE STUDY: THE MOSFET

3.1. TIA-based MOSFET current converter

A simple example of a TIA-based circuit is the current measurement schematic for a n-channel MOSFET (Fig. 2). The output signal's (V_o) linearity is directly dependent on the region of operation (linear/saturation, weak/strong inversion) and the varying voltage. In case the signal is applied on the gate, G, only the input characteristics (I_d-V_g) should be accounted for, whereas only the output ones (I_d-V_d) if the drain, D, carries the signal.

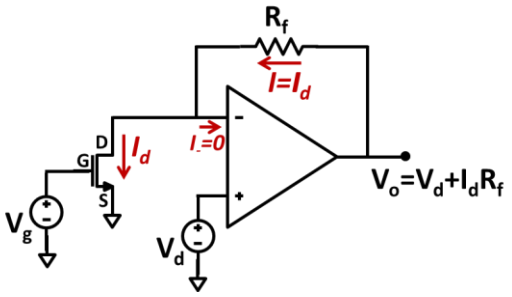

Figure 2: *Current-to-voltage converter configuration for MOSFET characterization (DC and noise)*

To understand the potential advantages for distortion, compared to a MOSFET amplifier, we underline that for the latter, the signal gain is also a function of the region of operation (linear/saturation) which affects the DC operating point and the load line. In fact, in order for the gain to be independent from the drain bias, the MOSFET in linear amplifiers is always biased in saturation, where -supposing a perfectly saturated current- the current is no more dependent on the drain voltage. In conclusion, for each DC bias and signal amplitude, one would obtain a specific set of harmonics, which only depends on the I-V transfer curves of the DUT and not in any other circuit elements, such as bias resistances as is the case in MOSFET amplifiers. This way, a high level of control and predictability over the generated distortion can be achieved, only by knowing the static (DC) behaviour of the electron device.

3.2. MOSFET modelling for simulations

In order to simulate the precise response of such a circuit, we need MOSFET models that are continuous and analytical from weak to strong inversion and from linear to saturation regimes. Thankfully, such a modelling approach exists and utilizes the Lambert-W (LW) function [12]-[13], which provides a very good description of the inversion charge behavior in all bias regions. This modelling approach is described by equations (5):

$$I_d = \frac{W}{L} \mu_{eff} \left[(q_s - q_d) + \frac{1}{2\eta k T C_{ox}} \left(q_s^2 - q_d^2 \right) \right] \tag{5a}$$

$$q_s = \eta k T C_{ox} L W \left(e^{(V_g - V_t)/\eta k T} \right) \tag{5b}$$

$$q_{\mathrm{d}} = \eta kTC_{ox}LW\left(e^{(V_g - V_t - V_{\mathrm{d}})/\eta kT}\right) \quad (5c)$$

where W, L the width and length of the channel, μ_{eff} the effective mobility, V_t the threshold voltage, η the sub-threshold ideality factor (=1 for 60mV/dec), kT the thermal voltage (≅26mV at room temperature), and C_{ox} the oxide capacitance per unit area. The quantities q_s and q_d represent the carrier charge densities near the source, S, and drain, D, of the transistor, respectively. Fig. 3 shows an example of input and output MOSFET transfer curves as calculated by (5), with W = 1 μm, L = 0.2 μm, V_t = 0.5 V, μ_{eff} = 100cm^2/Vs, C_{ox} = 1.2μF/cm^2, and η = 1.

The typical behavior of a MOSFET's drain current, I_d, with gate and drain bias voltages can be seen:

1) exponential increase with V_g below V_t (weak inversion), whereas linear above V_t (strong inversion) for low V_d values and quadratic for $V_d > V_g - V_t$, whereas
2) linear increase with V_d for $V_d << V_g - V_t$ (linear regime), constant current (saturation) for $V_d > V_g - V_t$, and logarithmic behavior between the two (triode region).

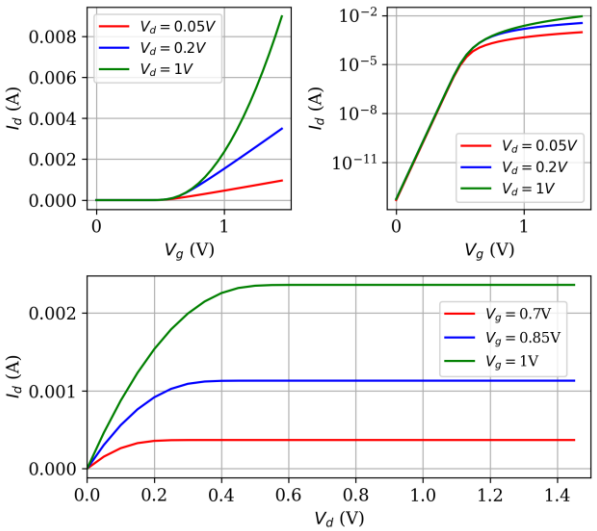

Figure 3: *Typical DC transfer characteristics for varying gate voltage (top/lin-log Y-scale) and drain voltage (bottom)*

Thanks to the simplicity of the proposed TIA-based circuit (Fig. 2), these curves are actually translated into voltage transfer functions (Fig. 4), because $V_0 = V_d + I_d R_f$. The R_f value is adapted so that the maximum voltage does not surpass the power supply of the OPAMP (+15V). The offset in high V_d values can be corrected by subtracting the DC bias of the drain from the output signal.

Consequently, depending on the DC bias around which we apply our signal, as well as the signal amplitude itself, we can expect very different results in terms of distortion. This is graphically demonstrated in Fig. 5, where an AC signal is applied at the MOSFET's gate, around 2 different DC bias (moderate and strong inversion) and with two different amplitudes. The first signal, oscillating around moderate inversion, is objected to the exponential dependence of $I_d(V_g)$, resulting in a signal with almost clipped bottom half and an exponentially distorted top half.

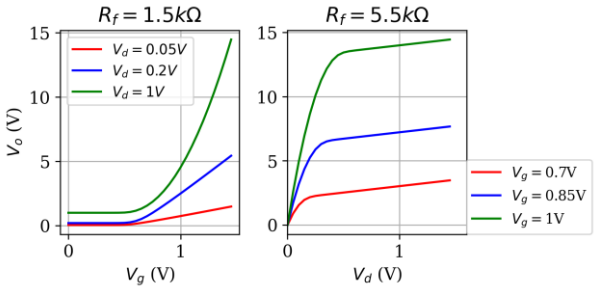

Figure 4: *Transfer characteristics of Fig.2's circuit with the I-V curves of Fig. 3.*

On the other hand, if we apply a signal around a V_g well above V_t, the signal has almost no distortion in linear region, while following a quadratic distortion in saturation (high V_d). It should be noted here that the signal amplitude was deliberately chosen to be significantly high, in order to capture the passage from weak to strong inversion and the quadratic dependence. If the signal amplitude is very small (mV range) and the DC bias is well above V_t, the distortion will be negligible.

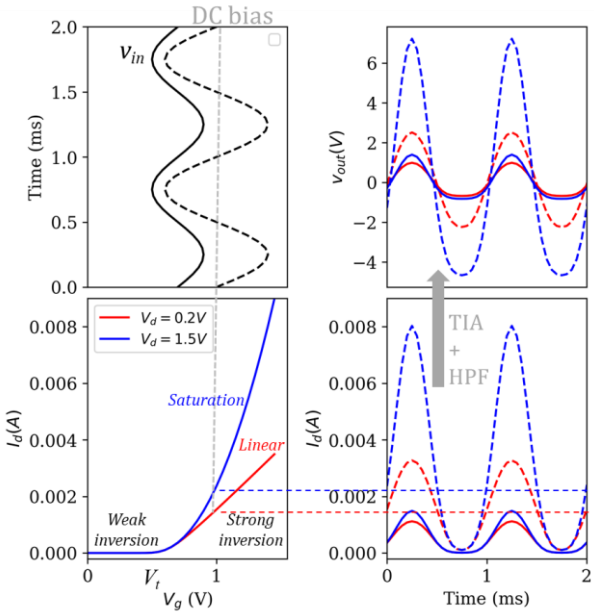

Figure 5: *Graphic demonstration of the distortion effect of the proposed circuit (Fig. 2), depending on the DC bias and AC amplitude of a signal applied at the transistor gate (TIA: Transimpedance amplifier, HPF: high-pass filter).*

3.3. Harmonic distortion analysis

Following the same simulation method, we examined many different scenarios of gate and drain DC bias and AC signal amplitudes, to reveal the variety of different harmonic content. Fig. 6 and Fig. 7 show two examples where both DC biases are kept constant at $V_g = V_d = 1$ V, but the signal (f = 1 kHz) is applied at the gate (Fig. 6) or at the drain (Fig. 7). The power spectra shown are obtained using the Welch periodogram method in SciPy (Python), whereas the signals have been normalized in amplitude so that they can be easily plotted and visualized together in the same

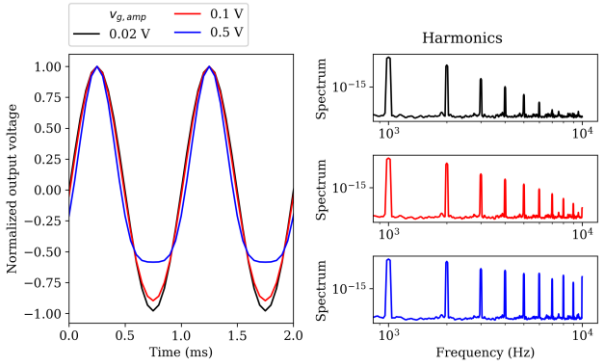

Figure 6: *Power spectrum calculations for the case where a signal is applied at the MOSFET gate for 3 different AC amplitudes. DC bias: V_g = V_d = 1 V.*

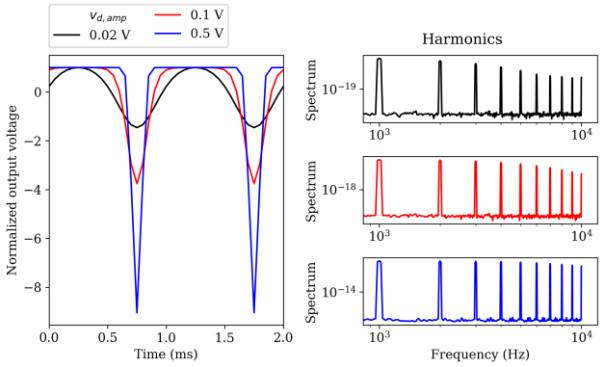

Figure 7: *Power spectrum calculations for the case where a signal is applied at the OPAMP's (+) input for 3 different AC amplitudes. DC bias: V_g = V_d = 1 V.*

graph; in any case, large amplitude differences can be compensated at the output thanks to R_f.

It becomes evident from Fig. 6 that when the signal amplitude is large enough to cover two different transistor operation regimes, it can dramatically affect the harmonic distortion. That's because in the case of varying V_g in saturation (Fig. 6), the signal is prone to the ~$(V_g$-$V_t)^2$ behavior of I_d, whereas varying V_d in strong inversion around 1 V (Fig. 7) can actually cause asymmetrical hard clipping of the signal due to the alternating between linear and triode regimes. As a result, the harmonic distortion in the latter case is much more severe, which is directly visible in the high amplitude of high-order harmonics.

We repeated this type of simulations for many combinations of DC biases V_g and V_d, from 0 up to 2 V, and various signal amplitudes, v_{amp}, from 50mV to 0.5V, and we extracted the power values of each harmonic in order to visualize their dependence with the applied voltages. Fig. 8 shows the relative (with regard to the fundamental's power) power of four harmonics (2nd to 5th) for v_{amp} = 0.5 V applied at the gate and Fig. 9 at the drain. For the case where the signal is around V_g (Fig. 8), a clear reduction of harmonic distortion with V_g is visible, whereas this reduction for the 2nd and 3rd harmonic can be cancelled out by high V_d bias. The 4th and 5th harmonic seem to have a negligible amplitude, except for the case of very low V_g values (weak inversion).

Concerning the case where the signal is applied at the drain (V_+ input of OPAMP), high V_d values can make the harmonic distortion immune to variations in V_g bias, and it is worth noting

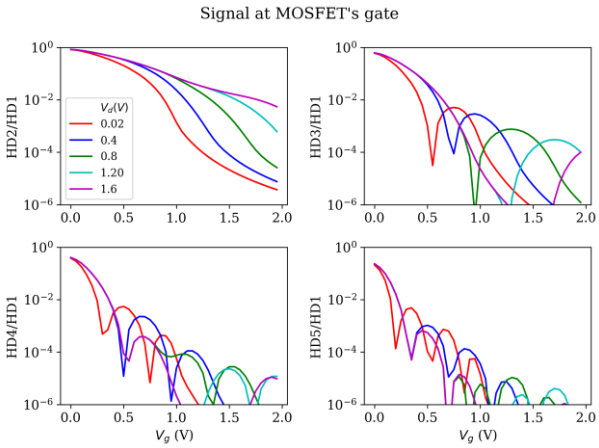

Figure 8: *Relative power levels of the 4 first harmonics for a signal of v_{amp} = 0.5 V amplitude applied at the gate, and various combinations of V_g and V_d DC bias.*

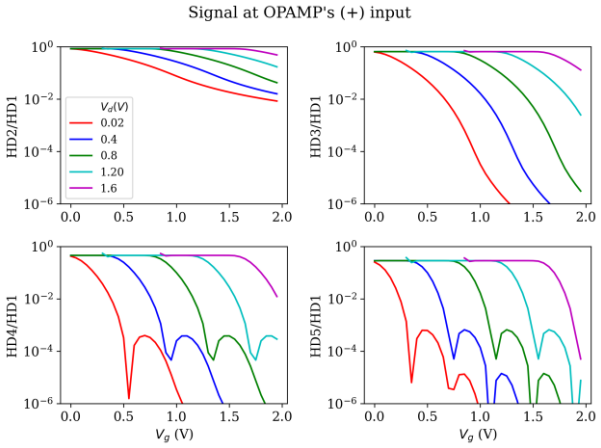

Figure 9: *Relative power levels of the 4 first harmonics for a signal of $v_{d,amp}$ = 0.5 V amplitude applied at (+), and various combinations of V_g and V_d DC bias.*

that here, even the 4th and 5th harmonics have very significant contributions.

By using formula (6), we also calculated the total harmonic distortion (THD) for various combinations of V_g and V_d, accounting up to the 5th harmonic.

$$\mathrm{THD}(\%) = 100\sqrt{\frac{\mathrm{HD2+HD3+HD4+HD5}}{\mathrm{HD1}}} \qquad (6)$$

where HDx the power of the xth harmonic. The results are plotted in Fig. 10, for v_{amp} = 0.2 V applied at the MOSFET's gate, and in Fig. 11 for the case where the signal is applied at the (+) input.

It is worth noting that in both cases (AC around V_g and around V_d), the THD reaches 100% for certain DC bias combinations, while it can also be decreased down to 0.1% for others. This is a direct confirmation of our hypothesis that with the circuit architecture of Fig. 2, any amount of THD can be achieved, provided that one examines all the possible bias conditions.

Moreover, the THD has a characteristic value for each combination of V_g, V_d and v_{amp}, making it easy to use this concept as the basis for a variety of audio distortion (or even tone control) applications. For example, as far as v_{amp} is concerned, Fig. 12

shows how it can impact THD when the signal is at the gate, for both linear (V_d = 0.1 V) and saturation (V_d = 2 V) regions. Similarly, in Fig. 13 is plotted the THD versus v_{amp} when the signal is at the (+) OPAMP's input, for both weak (V_g = 0.5 V) and strong (V_g = 1.5 V) inversion regions. As it can be seen, the THD is always increasing with v_{amp}, except when the DC bias is at weak inversion (V_g = 0.5 V), where THD reaches a plateau around v_{amp} = 0.2 V. Note also how there is no signal for V_d = 1.5 V in weak inversion, because the signal amplitude needed to reach triode region is higher than the maximum value of $v_{d,amp}$. Therefore the drain current is constant whatever the fluctuation of V_d.

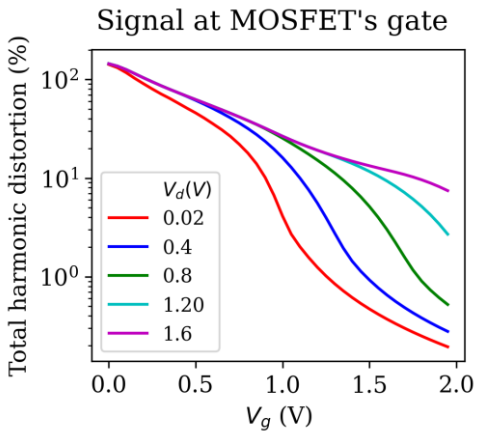

Figure 10: *THD for a signal of v_{amp} = 0.2 V amplitude applied at the gate, and various combinations of V_g and V_d DC bias.*

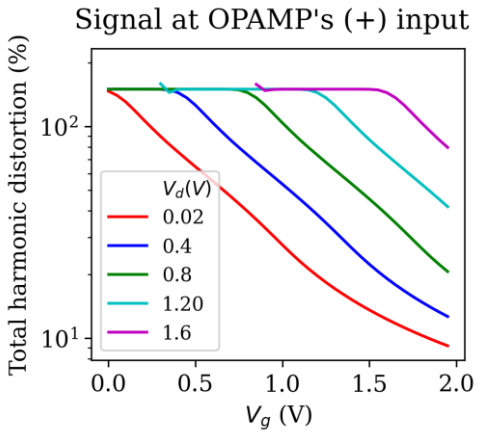

Figure 11: *THD for a signal of v_{amp} = 0.2 V amplitude applied at (+), and various combinations of V_g and V_d DC bias.*

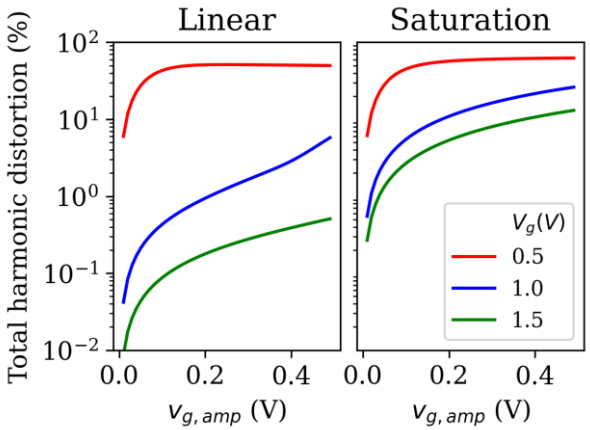

Figure 12: *THD versus varying signal amplitude v_{amp} applied at the MOSFET's gate, for linear (left) and saturation (right) regimes.*

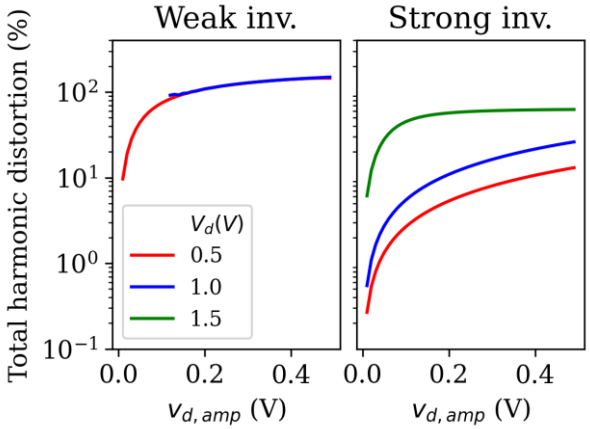

Figure 13: *THD versus varying signal amplitude v_{amp} applied at the OPAMP's (+) input, for weak (left) and strong (right) inversion regions.*

4. MEASUREMENT RESULTS

We constructed the circuit shown in Fig.2, using the Onsemi BS170 enhancement mode n-channel MOSFET as a device under test, which has a V_t around 2 V. Following the same methodology as in the simulations, we tested the output response for various V_g and V_d DC bias and signal amplitudes, with the signal applied at the MOSFET's gate. Some examples are shown in Fig. 14 (linear regime) and Fig. 15 (saturation regime). The value of Rf was modified for every case, in order to avoid OPAMP saturation or negligible output amplitude.

In Fig. 14 we note a verification of the bottom half soft clipping due to alternating from strong to weak inversion in linear region (as in Fig. 5), while in Fig. 15 the quadratic dependence of $I_d(V_g)$ in saturation regime gives a smooth distortion to the signal. For higher signal amplitudes, a more severe low-half clipping is visible, due to the passage to weak inversion (as in Fig. 6).

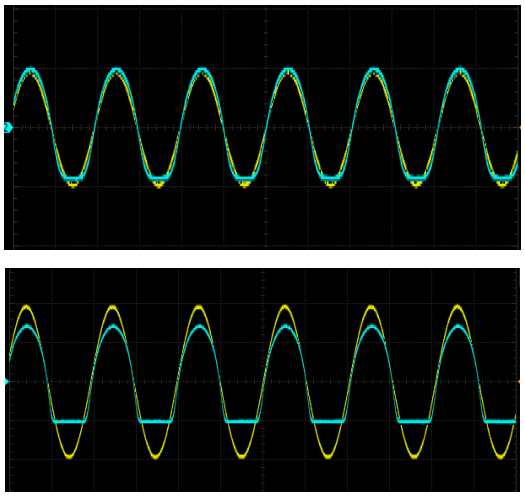

Figure 14: *Measured input (yellow) and output (blue) signals for V_d = 50 mV, V_g = 3 V, v_{amp} = 1 V (top) and 2 V (bottom) around gate voltage.*

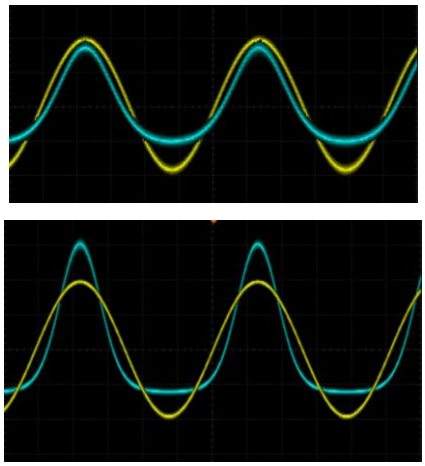

Figure 15: *Measured input (yellow) and output (blue) signals for V_d = 0.5 V, V_g = 2 V, v_{amp} = 0.1 V (top) and 0.2 V (bottom) around gate voltage.*

5. CONCLUSIONS

We have presented an analog circuit that can be used to exploit the non-linearities in any electron device, aiming the harmonic audio distortion. The n-channel MOSFET was shown and studied as an example, revealing a high level of control of the output signal harmonics through the DC gate and drain bias voltages, the signal's amplitude, as well as its input position (gate or drain). The effect was studied both through simulations and measurements. The proposed circuit configuration could be potentially used in guitar effect pedals or analog synthesizers.

6. REFERENCES

[1] T. Hamasaki, "Learn about harmonics by means of vacuum tube guitar amplifier," in *Proceedings of the AES International Conference*, 2013, pp. 98–102.

[2] K. Takemoto, S. Oshimo, and T. Hamasaki, "Supply voltage scaling technique of triode tube based on harmonic distortion characteristics," in *142nd Audio Engineering Society International Convention 2017, AES 2017*, 2017.

[3] R. C. D. Paiva, S. D'Angelo, J. Pakarinen, and V. Välimäki, "Emulation of operational amplifiers and diodes in audio distortion circuits," *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 59, no. 10, 2012,DOI:10.1109/TCSII.2012.2213358.

[4] J. D. Reiss and A. McPherson, "Overdrive, Distortion, and Fuzz," in *Audio Effects*, CRC Press, 2014, pp. 182–203.

[5] J.-M. Réveillac, *Musical Sound Effects*. Hoboken, NJ, USA: John Wiley & Sons, Inc., 2018.

[6] D. J. Dailey, *Electronics for Guitarists*. Springer Cham, 2013.

[7] W. Sansen, "Distortion in elementary transistor circuits," *IEEE Trans. Circuits Syst. II Analog Digit. Signal Process.*, vol. 46, no. 3, 1999,DOI:10.1109/82.754864.

[8] B. C. Paz *et al.*, "Non-linearity analysis of triple gate SOI nanowires MOSFETS," *SBMicro 2016 - 31st Symp. Microelectron. Technol. Devices Chip Mt. co-located 29th SBCCI - Circuits Syst. Des. 6th WCAS - IC Des. Cases, 1st INSCIT - Electron. Instrum. 16th SForum - Undergraduate-Stude*, pp. 3–6, 2016,DOI:10.1109/SBMicro.2016.7731355.

[9] A. Cerdeira, M. Estrada, R. Quintero, D. Flandre, A. Ortiz-Conde, and F. J. García Sánchez, "New method for determination of harmonic distortion in SOI FD transistors," *Solid. State. Electron.*, vol. 46, no. 1, pp. 103–108, 2002,DOI:10.1016/S0038-1101(01)00258-1.

[10] C. Beguni, A. M. Cailean, S. A. Avatamanitei, and M. DImian, "Photodiode Amplifier with Transimpedance and Differential Stages for Automotive Visible Light Applications," in *2020 15th International Conference on Development and Application Systems, DAS 2020 - Proceedings*, 2020.

[11] J. A. Chroboczek, A. Szewczyk, And G. Piantino, "Low Frequency Noise Point Probe Measurements On A Wafer Level Using A Novel Programmable Current Amplifier," in *Noise in Physical Systems and 1/f Fluctuations*, 2001, pp. 701–704.

[12] K. Papathanasiou *et al.*, "Symmetrical unified compact model of short-channel double-gate MOSFETs," *Solid. State. Electron.*, vol. 69, pp. 55–61, 2012.

[13] T. A. Karatsori *et al.*, "Full gate voltage range Lambert-function based methodology for FDSOI MOSFET parameter extraction," *Solid. State. Electron.*, vol. 111, 2015,DOI:10.1016/j.sse.2015.06.002.