ENHANCED DIGITAL MODELS FOR ANALOG MODULATION EFFECTS

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ABSTRACT

This paper presents digital models for analog phaser and flanger / chorus effects. The structure of analog phasers is reviewed. The operation of two phaser implementations is analyzed and nonlinear digital models are presented for them. The models are based on cascades of one-pole filters with embedded nonlinearities and are suitable for real-time implementation. Modifications to standard digital flanger / chorus effect are also presented. A method to warp the delay time to more closely resemble the behavior of bucket brigade delays is presented. Also a simple model for companders used in such analog effect units is presented.

1. INTRODUCTION

The term "modulation effect" generally means an audio effect where some parameter is changed (modulated) in a periodic fashion. This differs from the stricter signal processing interpretation, where modulation means some form of shifting the frequency spectrum of a signal [1]. The most common modulation effects are phaser, flanger and chorus, which will be dealt with in this paper. For more comprehensive treatise on audio effects, see [2].

A phaser, or a phase-shifter as it was originally called, generates a number of notches in the signal spectrum. The position of the notches is modulated by a Low Frequency Oscillator (LFO) using typically a sinusoidal or a triangle wave. The synchronized sweeping of the notches causes a characteristic "whooshin" sound. Phasers are popular among guitarists but they are also often used with synthesizers.

A flanger mixes a slightly delayed signal with the original, acting as a comb filter. This produces a large number of regularly placed notches in the spectrum. As the delay time is varied (again with an LFO), the notches move up and down in the spectrum, creating a somewhat similar sound to phaser. As the notches are spaced regularly and extend up to infinity, flangers tend to sound more metallic than phasers. Flangers often add feedback from delay output to input to produce a number of peaks to emphasize the effect.

For chorus, a longer delay is used. The ear perceives this as a doubling effect, giving the impression of several instruments playing at once (such as in a string ensemble for example). Vibrato can also be produced with a modulated delay, although it is not a very common effect. Vibrato is otherwise similar to flanger, but only the delayed signal is used.

1.1. Digital modulation effects

The phaser effect has been implemented digitally using time-varying allpass filters [3]. A number of allpass filters are placed in series and the phase shifted signal is mixed with dry signal. This results in notches (destructive interference) at frequencies where the phase shift of the allpass chain is $(1+2N)180$ degrees. This is similar to the analog approach, but as the allpass filters are second-order filters, the center frequency and the bandwidth can be independently controlled.

Digital flanger and chorus effects use fractional delay lines to produce a time varying delay [4]. Mixing the delayed signal with dry signal makes them essentially time-varying comb-filters. Adding feedback transforms the comb-filter from pure FIR to IIR comb-filter. Digital fractional delay lines have been extensively reviewed in [5].

Recently there has been interest in modeling specific analog circuits. Certain effect units are held in high regard for their characteristic sound. For example the Moog lowpass filter has been modeled in [6].

This paper presents a generic model for analog phaser effects, as well as two different implementations for the individual phase stages. The implementations model the inherent non-linearities of the analog circuits. All parameters of the digital model are based on values of the analog components, and thus no hand tuning is required.

Additions to existing flanger / chorus models are also suggested that alter the behavior to more closely resemble analog implementations. A separate variable speed delay line is used to model the delay-time behavior of analog bucket brigade delays. A method of warping the modulation curve of standard modulated delay is also presented for a simple approximation. Additionally, a model for a compander often present in such devices is shown.

2. ANALOG PHASERS

Figure 1 shows the structure of a typical analog phaser. Analog phasers have four or more first-order allpass filters connected in series whose output is mixed with the input. Each allpass filter generates a total phase shift of 180 degrees, producing one notch for every two stages. Modulating the center frequencies with an LFO moves the notches in frequency and produces the characteristic swooshing sound. Typically the sound is accentuated by feeding back some of the unmixed allpass chain output to produce one or more frequency peaks in the spectrum.
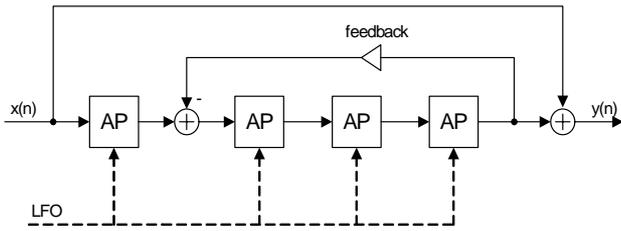
Figure 1: *Structure of typical analog phaser.*

A digital model likewise uses four or more allpass filters in series. First-order digital allpass filters are used to preserve the allpass nature of the circuit. If a specific analog circuit is to be emulated, the center frequencies should be selected to match it's properties. The feedback is also implemented in the same way, but a unit delay is inserted to make the structure realizable. This causes the frequencies of the resonances to differ from those of the analog circuit, but as the feedback amount is typically low the difference can likely be ignored.

The allpass filters can be implemented by several different methods [7]. Early designs, such as the Uni-Vibe, used light dependent resistors to alter the cutoff frequency of an RC-circuit. Later in the 70s, Field Effect Transistors (FETs) were used as voltage controlled resistors in units such as MXR Phase90. Electro-Harmonix Small Stone phaser used Operational Transconductance Amplifiers (OTAs). Even pulse-width modulation has been used to imitate a voltage controlled resistor (the technique is similar to switched-capacitor filters).

The FET and OTA circuits will be analyzed in closer detail next.

3. OTA ALLPASS STAGE

Figure 2 shows a schematic of an OTA based allpass stage [7]. An Operational Transconductance Amplifier produces output current that is the product of control current I_{ctrl} and voltage between the V_+ and V_- input terminals [8]. In the circuit, the OTA is used as a voltage controlled resistor, which sets the center frequency in combination with capacitor C. Resistors R1 sum the input voltage and the buffered capacitor output voltage while resistor R2 attenuates this combined voltage suitable for the OTA input.
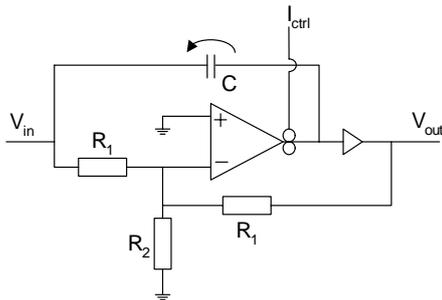
Figure 2: *Schematic for OTA allpass filter circuit.*

3.1. Differential equation for OTA allpass stage

The OTA output current is given [8] by

$$I = I_{ctrl} \tanh\left(\frac{V_+ - V_-}{2V_t} \right), \qquad (1)$$

where V_+ and V_- are the voltages at the OTA input terminals and V_t is the thermal voltage of a transistor [9] (typically 25 mV at room temperature). As V_+ is connected to ground, this can be written as

$$I = I_{ctrl} \tanh\left(\frac{-R_2\left(2V_{in} + V_c\right)}{2R_1 V_t} \right). \qquad (2)$$

The differential equation for voltage over capacitor C is then

$$\frac{dV_c}{dt} = \frac{I_{ctrl}}{C} \tanh\left(\frac{-R_2\left(2V_{in} + V_c\right)}{2R_1 V_t} \right). \qquad (3)$$

We leave the solution in this form as it results in a simpler discrete time model instead of writing the equation in terms of input V_{in} and output V_{out}.

3.2. Difference equation for OTA allpass stage

This differential equation can be solved using Euler's method to produce a digital difference equation. To simplify the process, we use an extra variable $w(n)$ to denote the voltage over capacitor C. Euler's solution for Eq. (3) is

$$w(n) = w(n-1) + \frac{I_{ctrl}}{Cf_s} \tanh\left(\frac{-R_2\left(2x(n) + w(n-1)\right)}{2R_1 V_t} \right), \quad (4)$$

where x_n is the input signal and f_s is the sampling rate. The final output is then

$$y(n) = x(n) + w(n) . \qquad (5)$$

For small signals the tanh-function can be considered linear and the difference equation behaves as a first-order digital filter. When analyzed, the filter has two flaws. The filter only approaches allpass for low center frequencies with substantial low-pass effect appearing with high center frequencies. Substituting $x(n)+x(n-1)$ for $2x(n)$ in Eq. (4) makes the filter true allpass.

Another problem is the non-linear tracking of center frequency to control current unlike with the analog version. This can be remedied by observing that, for small signals, Eq. (4) is very similar to the scaled impulse invariant transformed one-pole low-pass filter [10].

Figure 3 shows the corrected filter structure.
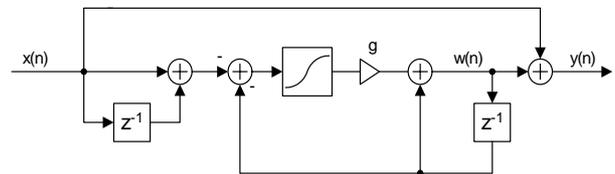
Figure 3: *Digital model of an OTA allpass filter circuit.*

The corrected difference equation is

$$w(n) = w(n-1) + \frac{2R_1 V_t g}{R_2} \tanh\left(\frac{-R_2 \left(x(n) + x(n-1) + w(n-1)\right)}{2R_1 V_t}\right) \quad (6)$$

$$y(n) = x(n) + w(n) \quad (7)$$

$$g = 1 - \exp\left(-2\pi \frac{f_c}{f_s}\right). \quad (8)$$

4. JFET ALLPASS STAGE

Figure 4 shows the schematic for a first-order allpass filter where a JFET-transistor is used as voltage controlled resonance [7]. Resistor R_p is inserted in parallel with the JFET to ensure that the signal is never completely cut off. Control voltage V_g determines center frequency along with capacitor C. The two resistors R along with the operational amplifier form the rest of the circuit.
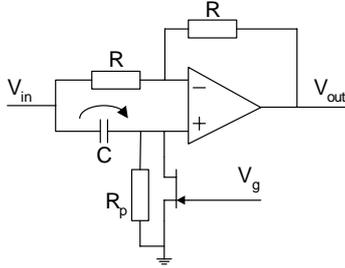
Figure 4: *Schematic for FET allpass filter circuit.*

4.1. Differential equation for JFET allpass stage

A JFET transistor has the following current-voltage characteristic

$$I_{ds} = \frac{I_{DSS}}{V_p^{\ 2}} \left[2\left(V_{gs} - V_p\right)V_{ds} - V_{ds}^{\ 2}\right], V_{ds} \leq V_{gs} - V_p \quad (9a)$$

$$I_{ds} = \frac{I_{DSS}}{V_p^{\ 2}} \left(V_{gs} - V_p\right)^2 \left(1 + \lambda V_{ds}\right), V_{ds} > V_{gs} - V_p, \quad (9b)$$

where I_{ds} is the current through JFET, I_{DSS} is the drain-source saturation current (manufacturing constant, typically around 1 mA), V_{gs} is the voltage between the gate and the source terminals, V_{ds} the voltage between the drain and the source, V_p is the pinch-off voltage of the JFET (also a manufacturing constant, typically –1 V to –5 V) and λ depends on the so-called Early-voltage [9]. λ is typically very small and can in this case be safely ignored.

Figure 5 shows the I_{ds}-V_{ds} transfer curve of a typical JFET transistor ($V_p = -3$ V, $I_{DSS} = 1$ mA). The nonlinearity can be clearly seen, especially for low V_g.

The voltages at the operational amplifier terminals are

$$V_+ = V_{in} - V_c \quad (10)$$

$$V_- = V_+ \quad (11)$$

$$V_{out} = V_+ - \frac{V_{in} - V_+}{R} R = V_{in} - 2V_c. \quad (12)$$
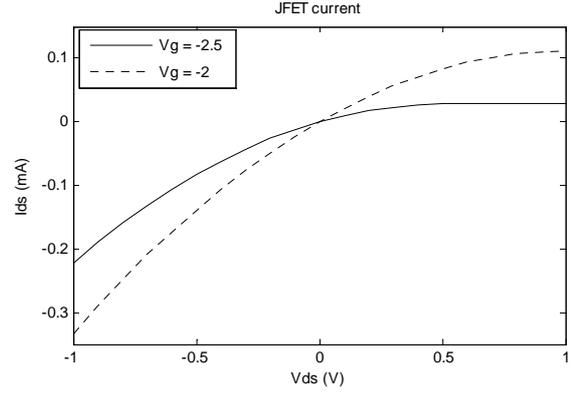
Figure 5: *JFET transfer curve.*

Eq. (9) can now be written as

$$I_{ds} = \frac{I_{DSS}}{V_p^{\ 2}} \left[2\left(V_g - V_p\right)V_+ - V_+^{\ 2}\right] \quad V_+ \leq V_g - V_p \quad (13a)$$

$$I_{ds} = \frac{I_{DSS}}{V_p^{\ 2}} \left(V_g - V_p\right)^2 \quad V_+ > V_g - V_p \quad (13b)$$

As V_g and V_+ are the only non-constant terms in Eq. (13), we will use $I_{ds}(V_+, V_g)$ in its place. The current through capacitor C is then

$$I_c = C\frac{dV_c}{dt} = \frac{V_+}{R_p} + I_{ds}(V_+, V_g). \quad (14)$$

For small signals

$$I_{ds} \approx 2\frac{I_{DSS}}{V_p^{\ 2}}\left(V_g - V_p\right)V_+ \quad (15)$$

$$\frac{dV_c}{dt} = \frac{1}{C}\left(\frac{1}{R_p} + 2\frac{I_{DSS}}{V_p^{\ 2}}\left(V_g - V_p\right)\right)V_+. \quad (16)$$

Some phasers used a method of linearizing the JFETs by feeding some of the drain signal to the gate. For these circuits, equation (16) should be used.

From equations 14-16, it can be seen that the center frequency is

$$f_c = \frac{1/R_p + 2\frac{I_{DSS}}{V_p^{\ 2}}\left(V_g - V_p\right)}{2\pi C}, \quad (17)$$

which will prove to be useful for a discrete-time model of FET phase stage.

4.2. Difference equation for JFET allpass stage

For discretization of equation 14 we again introduce a temporary variable w_n denoting the voltage over capacitor C. Euler solution for Eq. (14) is

$$u(n) = x(n) - w(n-1), \quad (18)$$

$$w(n) = w(n-1) + \frac{1}{Cf_s}\left(\frac{1}{R_p}u(n) + I_{ds}(u(n), V_g)\right). \quad (19)$$

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The final output is then

$$y(n) = x(n) - 2w(n).\qquad(20)$$

This difference equation suffers from the same problems as the first attempt for OTA-based phaser stage. The stage is easily converted to true allpass filter by splitting $2w_n$ in Eq. (20) so that

$$y(n) = x(n) - w(n) - w(n-1).\qquad(21)$$

Figure 6 shows the corrected FET allpass stage.
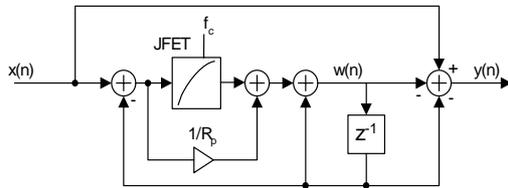
Figure 6: *Digital model of a FET allpass filter.*

The filter still suffers from the digital warping of center frequency. w_n is seen to be a first-order lowpass filter. For a lowpass filter in the form

$$y(n) = y(n-1) + g(x(n) - y(n-1)),\qquad(22)$$

coefficient g can be calculated with

$$g = 1 - \exp(-2\pi f_c/f_s).\qquad(23)$$

Then if R_p is held constant, the center frequency of the digital allpass filter can be corrected by scaling I_{ds} so that

$$2\frac{I_{DSS}}{V_p{}^2 Cf_s}\left(V_g - V_t\right) - \frac{1}{R_p Cf_s} = 1 - \exp(-2\pi f_c/f_s).\qquad(24)$$
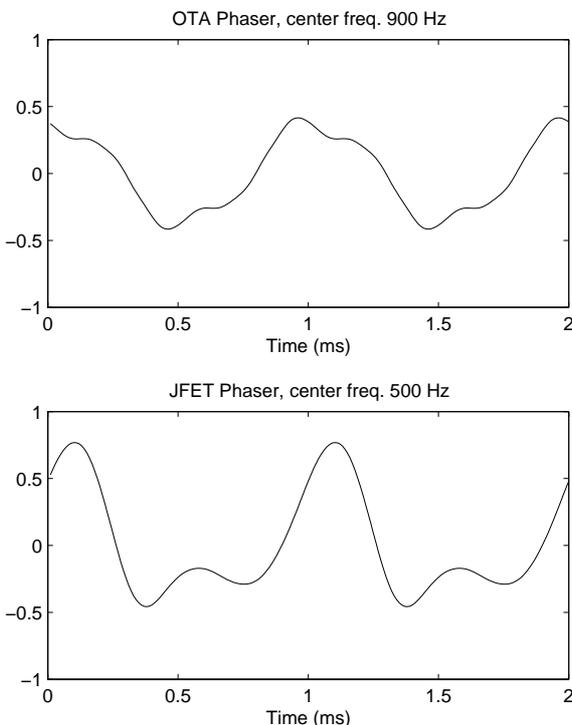
Figure 7: *Comparison of OTA and JFET phasers for sinusoidal input.*

4.3. Comparison of OTA and JFET phasers

Figure 7 shows the output from the two phaser models for a single sinusoidal input. The frequency of the input sinusoidal is 1000 Hz. The input amplitude is higher than usual to better illustrate the effects of the nonlinearities.

The center frequencies of the phasers have been selected to better show the generated harmonics by placing a notch at the sinusoidal frequency. The symmetric distortion in OTA lowers the gain and thus center frequency. Therefore the actual center frequency has been adjusted to match that of the JFET phaser.

5. ANALOG FLANGER AND CHORUS

The flanger is a close relative of the phaser effect. While phaser produces a constant limited number of notches in the spectrum, the flanger produces infinitely many notches that are spaced at constant intervals. The flanger works by mixing a delayed copy with the original signal and modulating the delay time. As such, the flanger is a special case of a comb filter. Typical delay times are around a few milliseconds. If the delay time is increased to tens of milliseconds, ear perceives the effect as an additional voice, producing a chorus effect.

Analog delays are realized with so-called Bucket Brigade Delay (BBD) chips [11]. These have a large number of capacitors in series with switches between them. An external clock is used to turn on and off the switches and thus propagate the signal within the chip. As the number of capacitors, or taps as they are called, is fixed, the delay time is changed by varying the clock.

While a BBD delay is analog and does not quantize the signal like digital delays, it still samples the signal. Therefore, proper anti-aliasing and anti-imaging filters are required before and after the delay IC. These are typically 2nd to 4th order filters. The output anti-imaging filter also serves to filter out the considerable clock bleed-through noise.

Because BBD delays have a large number of stages in series through which the signal is propagated, the signal-to-noise ratio is typically poor. This is especially true for longer delays, such as those used in chorus effects. To alleviate this, the circuits often contain a compander, which contains a matched compressor and expander. The compressor is placed before the BBD delay and the expander after. Figure 8 shows the structure of a typical system using a BBD delay line.
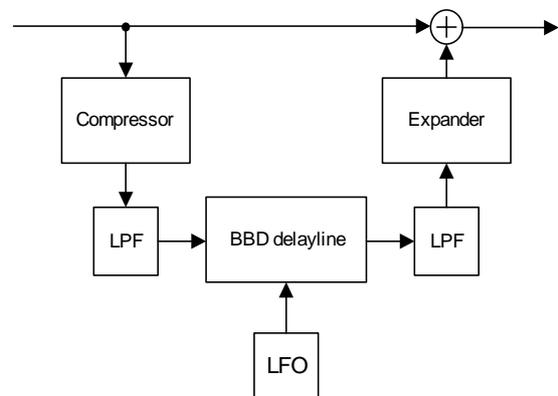
Figure 8: *Structure of analog flanger / chorus circuit.*

5.1. Simulating a BBD delay line

A BBD delay line differs from a digital delay in several ways. The most obvious is the limitation of constant length and severely limited output tap choices (typically only one). BBDs also suffer from heavy clock bleed-through at the output, attenuation of high frequencies, distortion and generally poor signal-to-noise ratio. Emulating these latter artifacts would require intimate knowledge of the BBD chip internals and likely heavy computation. For these reasons we limit our simulation to modeling only the limit on constant delay line length.

As the delay line length is fixed, the delay time can be varied only by changing the clock rate. This is equivalent to changing the sample-rate with time and has two effects: First, if the clock rate is varied linearly, the delay time will be roughly proportional to $1/x$. Second, as the clock-rate changes, the output sample-rate is not the same as the rate the audio was sampled in to the BBD. This causes some warping of the delay-time curve, especially if there are fast transitions or abrupt changes in the clock rate. Note that, unlike with digital delays, discontinuities in the modulating signal do not produce discontinuities in the delay time.

Figure 9 shows the delay time curves for BBD and digital delay in a chorus effect. Both BBD and digital delay are modulated with 2.5 Hz triangle wave and their minimum and maximum delay times are matched. The warping of the BBD delay-time is clearly visible.
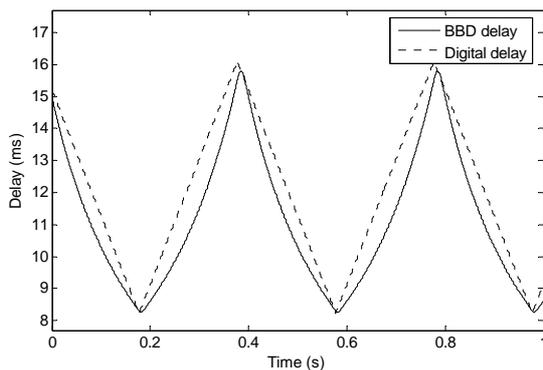
Figure 9: *Delay time of a BBD and a digital delay.*

A straightforward emulation of a BBD delay line would consist of resampling the input audio to BBD delay line. The BBD output would likewise be resampled back to DSP samplerate. This is obviously a very costly operation. Most resampling methods require some lookahead, which will additionally complicate matters. An alternative is to store time positions instead of samples in the BBD delay. Figure 10 shows the process.
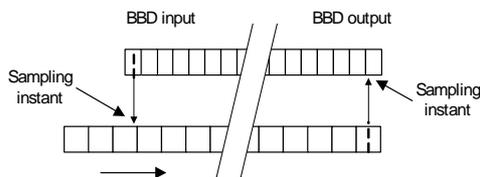
Figure 10: *Digital simulation of a BBD delay line.*

For each sample, the BBD output is sampled to find the stored time position. Current time is subtracted from the stored time and the result is used to address a conventional fractional delay line to produce the final output. After this, the BBD delay line position is advanced f_{clock}/f_s bins. If this counter rolls over one or more bins, the time positions of the roll-overs are stored in those bins.

Compared to the naïve resampling algorithm, this method can use linear interpolation for evaluating the time positions. For the final output any fractional delay algorithm can be used. These have been heavily researched, with a good overview given in [5]. The computational cost is then the cost of fractional delay and calculating the time positions. Calculating the position for output sample requires just a single multiply (for linear interpolation). However, calculating the time position of each bin requires a division and a multiply. If several bins fall within a single sample, the positions of additional bins can be calculated by simple addition. Therefore the total cost is approximately one division, two multiplies and some additions per sample.

One might ask if it was possible to still reduce the computational cost. For an N tap BBD, as the clock rate f_{clock} approaches constant, the delay time t_d becomes

$$t_d = \text{avg}\left(\frac{N}{f_{clock}}, \frac{Nf_s}{f_{clock}}\right), \tag{25}$$

where $\text{avg}(x, M)$ is an M-point moving average filter. As the length of the moving average filter is fractional and varies with the clock rate, the equation does not produce exact results. However, as the main effect on the delay time is some smoothing, the remaining inaccuracy is unlikely to be significant if f_{clock} is replaced by its average value when calculating M. This modified algorithm then requires only a single division, a single multiplication and two additions per sample.

5.2. Compander model

As mentioned before, the BBD delays have a poor SNR. This gets worse as the number of taps is increased and the clock rate decreased, so circuits that use long delays often contain a compander to increase the SNR. A compander consists of a matched compressor to reduce the dynamic range before a low SNR transmission path and a matched expander to restore the dynamics back to original. For more detailed discussion on workings of compressors and expanders, see [2].

One such common IC is NE570 [12]. The circuit contains two matched 1:2 expanders, each having a precision full-wave rectifier with averaging capacitor, a variable gain amplifier and an op-amp. A 1:2 expander has the transfer function

$$y = \text{avg}(|x|)x . \tag{26}$$

As the input drops by 6 dB, the average also drops by same amount, resulting in a total drop of 12 dB, hence 1:2 expansion. Similarly as the input increases, the gain increases by the same amount. If such expander is placed in the feedback loop of an op-amp, the transfer function becomes

$$y = \frac{x}{\text{avg}(|y|)} . \tag{27}$$

By series expansion, it can be seen that for a constant input, the gain approaches $\sqrt{2}$, resulting in a 2:1 compressor.

The averaging is accomplished by a full-wave rectifier, two resistors and a capacitor in the NE570. Figure 11 shows an equivalent circuit for the averager.
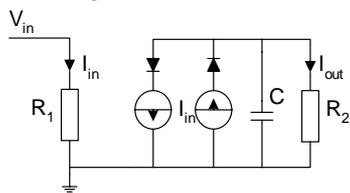
Figure 11: *Schematic of the averager in NE570.*

The differential equation for voltage over capacitor C is

$$\frac{dV_c}{dt} = \frac{1}{C}\left(\left|\frac{V_{in}}{R_1}\right| - \frac{V_c}{R_2}\right), \qquad (28)$$

where R_1 is the input gain resistor and R_2 is an internal resistor ($10k\Omega$). Equation (27) can be written as

$$\frac{dV_c}{dt} = \frac{1}{R_2C}\left(\frac{R_2}{R_1}\left|V_{in}\right| - V_c\right), \qquad (29)$$

making it obvious to be a lowpass filter with cutoff frequency

$$f_c = \frac{1}{2\pi R_2 C}, \qquad (30)$$

and gain

$$G = \frac{R_2}{R_1}. \qquad (31)$$

The compander can therefore be trivially modeled by equations (26) and (27) and two first-order lowpass filters.

6. CONCLUSIONS

Operation of analog phasers has been reviewed and digital models have been presented for two different analog phase stages. The phase stages have been shown to be first-order allpass filters with embedded nonlinearities, resulting in a simple digital implementation. The models can be used to emulate various different analog phaser effects with only minor parameter changes and possible modifications to the overall effect structure. As the phase stages contain nonlinearities, some oversampling is required. Informal tests suggest that two to four times oversampling is enough for almost all cases. The oversampling also helps to reduce any mismatch in the position of feedback resonances.

Additionally, a simple model has been shown for modeling some characteristics of analog delay based effects, such as flangers, choruses and delays. The model works together with traditional fractional delay line techniques, resulting in more accurate delay time behaviour. The model requires only a small number of additional operations making it well suited for real-time systems. A model for companders often present in such effects is also shown. The model is equivalent to simple expander and compressor and two first order lowpass filters requiring only minimal computation.

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